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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/563,630	03/06/2006	Hiroshi Fujioka	113184-114	1962
29175	7590	09/28/2006	EXAMINER	
BELL, BOYD & LLOYD, LLC P. O. BOX 1135 CHICAGO, IL 60690-1135			GOODWIN, DAVID J	
			ART UNIT	PAPER NUMBER
			2818	

DATE MAILED: 09/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/563,630

Applicant(s)

FUJIOKA ET AL.

Examiner

David Goodwin

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 May 2006.
- 2a) ☐ This action is **FINAL**.
- 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06 January 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☒ All b) ☐ Some * c) ☐ None of:
 - 1. ☒ Certified copies of the priority documents have been received.
 - 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 - 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 1/6/06
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

1.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 6, 7, and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Yano (US 6,045,626).

4. Regarding claim 1.

5. Yano teaches a semiconductor device. Said device comprises a substrate of yttria stabilized zirconia (21) (column 10 lines 30-60). Said YSZ layer preferably having a <111> orientation. A surface layer (22) wurzite, which has a hexagonal system; is formed on the surface and has a crystal structure being oriented with the c-axis thereof approximately vertical with respect to the <111> plane of said YSZ (fig 1a) (column 12 lines 55-60). Said wurzite may comprise InN (column 4 lines 25-40).

6. Regarding claim 2.

7. The surface of the YSZ layer (21) has a surface roughness of 0.6nm (column 9 lines 1-10). Said surface roughness consists of atomic level differences in surface elevation, atomic steps.

8. Regarding claim 6.

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9. Yano teaches a method of making a semiconductor device having a nitride semiconductor layer formed of InN. Said method comprises providing a substrate of yttria stabilized zirconia (21) (column 10 lines 30-60). Said YSZ layer preferably having a <111> orientation. A surface layer (22) comprising wurzite, which has a hexagonal system, is formed on the surface and has a crystal structure being oriented with the c-axis thereof approximately vertical with respect to the <111> plane of said YSZ (fig 1a) (column 12 lines 55-60). Said wurzite may comprise InN (column 4 lines 25-40).

10. Yano further teaches that the surface layer may be formed by physical vapor deposition, sputtering (column 16 lines 20-40).

11. Regarding claim 7.

12. Said wurzite surface layer (22) comprises InN (column 4 lines 25-40). Said layer being formed epitaxially by physical vapor deposition (column 16 lines 20-40).

13. Regarding claim 17.

14. The surface of the YSZ layer (21) has a surface roughness of 0.6nm (column 9 lines 1-10). Said surface roughness consists of atomic level differences in surface elevation, atomic steps.

15. Claims 3 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Kadota (US 6,291,257)

16. Regarding claim 3.

17. Kadota teaches semiconductor device. Said device comprises a ZnO substrate (3) and a nitride semiconductor layer including a GaN crystal layer (4) thereon (fig 1)

(column 4 lines 30-50). Gallium nitride has a hexagonal crystal structure. Said gallium nitride is aligned with the under lying crystal structure (fig 2). The ZnO layer is oriented in the c-axis direction, perpendicular to the <0001> plane, and so is the overlying gallium nitride.

18. Regarding claim 5.

19. Kadota teaches that the overlying layer comprises GaN (column 3 lines 1-30). Gallium nitride has the formula of $\text{In}_x\text{Ga}_{1-x}\text{N}$ (where $x=0$). Said gallium nitride is aligned with the under lying crystal structure (fig 2). The ZnO layer is oriented in the c-axis direction, perpendicular to the <0001> plane, and so is the overlying gallium nitride.

20.

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

22. Claims 8, 9, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yano (US 6,045,626) as applied to claim 7 above and further in view of Hosono (US 6,806,503).

23. Regarding claim 8.

24. Yano teaches elements of the claimed invention above in the rejection of claim 7.

25. Yano further teaches that the surface layer, InN, may be formed by physical vapor deposition, sputtering (column 16 lines 20-40).

26. Yano does not teach a step of forming an atomic step in advance on said $\langle 111 \rangle$ plane of said YSZ.

27. Hoosono teaches a method of making a semiconductor device comprising forming a YSZ layer. Said YSZ layer, having a $\langle 111 \rangle$ orientation, is heated to over 800 degrees which forms atomic levels steps on the substrate (column 9 lines 5-40).

28. It would have been obvious to one of ordinary skill in the art to heat the YSZ layer to over 800 degrees in order to improve the planarity of the layer.

29. Regarding claim 9.

30. Hoosono teaches a method of making a semiconductor device comprising forming a YSZ layer. Said YSZ layer, having a $\langle 111 \rangle$ orientation, is heated to over 800 degrees which forms atomic levels steps on the substrate (column 9 lines 5-40).

31. It would have been obvious to one of ordinary skill in the art to heat the YSZ layer to over 800 degrees in order to improve the planarity of the layer.

32. Regarding claim 19.

33. Hoosono teaches a method of making a semiconductor device comprising forming a YSZ layer. Said YSZ layer, having a $\langle 111 \rangle$ orientation, is heated to over 800 degrees which forms atomic levels steps on the substrate (column 9 lines 5-40).

34. It would have been obvious to one of ordinary skill in the art to heat the YSZ layer to over 800 degrees in order to improve the planarity of the layer.

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35. Claims 10, 11, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota (US 6,291,257) in view of Nanishi (US 6,146,916).

36. Regarding claim 10.

37. Kadota teaches a method of making a semiconductor device.

38. Said method comprises providing a ZnO substrate (3) and a nitride semiconductor layer including a GaN crystal layer (4) thereon (fig 1) (column 4 lines 30-50). Gallium nitride has a hexagonal crystal structure. Said gallium nitride is aligned with the under lying crystal structure (fig 2). The ZnO layer is oriented in the c-axis direction, perpendicular to the <0001> plane, and so is the overlying gallium nitride.

39. Kadota does not teach the method by which the gallium nitride layer is deposited.

40. Nanishi teaches a method of depositing a gallium nitride layer (43) on a zinc oxide substrate (42). Said method comprises a physical vapor deposition, sputtering, at 200 degrees column 6 lines 1-5).

41. It would have been obvious to one of ordinary skill in the art to deposit GaN at 200 degrees in order to avoid softening and deformation of the substrate during deposition which may occur at elevated temperatures.

42. Regarding claim 11.

43. Kadota teaches that the layers are grown epitaxially (fig 2) (column 4 lines 30-45).

44. Nanishi teaches a method of depositing a gallium nitride layer (43) on a zinc oxide substrate (42). Said method comprises an epitaxial deposition (column 5 lines

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50-55) using a physical vapor deposition, sputtering, at 200 degrees (column 6 lines 1-5).

45. It would have been obvious to one of ordinary skill in the art to use a physical vapor deposition in order to be able to use a low temperature process that will not damage the underlying layers during the deposition.

46. Regarding claim 15.

47. Nanishi teaches a method of depositing a gallium nitride layer (43) on a zinc oxide substrate (42). Said method comprises an epitaxial deposition (column 5 lines 50-55) using a physical vapor deposition, sputtering, at about 200 degrees (column 6 lines 1-5). The process will take place at the ambient temperature of the reactor.

48. It would have been obvious to one of ordinary skill in the art to use a physical vapor deposition in order to be able to use a low temperature process that will not damage the underlying layers during the deposition.

49. Regarding claim 16.

50. Kadota teaches semiconductor device. Said device comprises a ZnO substrate (3) and a nitride semiconductor layer including a GaN crystal layer (4) thereon (fig 1) (column 4 lines 30-50). Gallium nitride has a hexagonal crystal structure. Said gallium nitride is aligned with the underlying crystal structure (fig 2). The ZnO layer is oriented in the c-axis direction, perpendicular to the $\langle 0001 \rangle$ plane, and so is the overlying gallium nitride. The overlying layer comprises GaN (column 3 lines 1-30). Gallium nitride has the formula of $\text{In}_x\text{Ga}_{1-x}\text{N}$ (where $x=0$). Said gallium nitride is aligned

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with the underlying crystal structure (fig 2). The ZnO layer is oriented in the c-axis direction, perpendicular to the <0001> plane, and so is the overlying gallium nitride.

51. Nanishi teaches a method of depositing a gallium nitride layer (43) on a zinc oxide substrate (42). Said method comprises an epitaxial deposition (column 5 lines 50-55) using a physical vapor deposition, sputtering, at 200 degrees (column 6 lines 1-5).

52. It would have been obvious to one of ordinary skill in the art to use a physical vapor deposition in order to be able to use a low temperature process that will not damage the underlying layers during the deposition.

53.

54. Claims 12, 13, 18, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota (US 6,291,257) in view of Nanishi (US 6,146,916) as applied to claim 10 above, and further in view of Hosono (US 6,806,503).

55. Regarding claim 12.

56. Kadota in view of Nanishi teaches elements of the claimed invention above.

57. Nanishi teaches a method of depositing a gallium nitride layer (43) on a zinc oxide substrate (42). Said method comprises an epitaxial deposition (column 5 lines 50-55) using a physical vapor deposition, sputtering, at 200 degrees (column 6 lines 1-5).

58. Kadota in view of Nanishi does not teach a step that will form atomic level steps on the surface of the layer.

59. Hosono teaches submitting a ZnO layer to an anneal of 800 degrees to improve the surface smoothness of the layer resulting in atomic level steps.

60. It would have been obvious to one of ordinary skill in the art to anneal the ZnO layer in order to improve the smoothness of the layer.

61. Regarding claims 13, 18, and 20.

62. Hosono teaches submitting a ZnO layer to an anneal of 800 degrees to improve the surface smoothness of the layer resulting in atomic level steps.

63. It would have been obvious to one of ordinary skill in the art to anneal the ZnO layer in order to improve the smoothness of the layer.

64. Claims 4, 14 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadota (US 6,291,257) in view of Nanishi (US 6,146,916) in view of Hosono (US 6,806,503) as applied to claim 12 above, and further in view of Hosono (US 2005/0039670).

65. Regarding claims 4, 14 and 21.

66. Kadota (US 6,291,257) in view of Nanishi (US 6,146,916) in view of Hosono (US 6,806,503) teaches elements of the claimed invention above.

67. Kadota (US 6,291,257) in view of Nanishi (US 6,146,916) in view of Hosono (US 6,806,503) does not teach surrounding the zinc oxide layer with a zinc containing material.

68. Hosono (US 2005/0039670) teaches a method of making a semiconductor device comprising encircling zinc containing material during an annealing step (paragraph 0067).

69. It would have been obvious to one of ordinary skill in the art to surround the layer with a zinc containing material in order to increase the partial pressure of zinc in the atmosphere thereby reducing the evaporation of zinc from the layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Goodwin whose telephone number is (571)272-8451. The examiner can normally be reached on Monday through Friday, 9:00am through 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571)272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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DJG

Andy Nguyen
Primary Examiner